

1 Alan P. Block (SBN 143783)  
2 ablock@mckoolsmith.com  
3 **MCKOOL SMITH, P.C.**  
4 300 South Grand Avenue, Suite 2900  
5 Los Angeles, California, Suite 2900  
6 Telephone: (213) 694-1200  
7 Facsimile: (213) 694-1234

8 Paul Richter\*  
9 **DEVLIN LAW FIRM LLC**  
10 1526 Gilpin Avenue  
11 Wilmington, Delaware 19806  
12 Telephone: (302) 449-9010  
13 Facsimile: (302) 353-4251

14 David Sochia\*  
15 dsochia@McKoolSmith.com  
16 Ashley N. Moore\*  
17 amoore@McKoolSmith.com  
18 Richard A. Kamprath\*  
19 rkamprath@McKoolSmith.com  
20 Alexandra Easley\*  
21 aeasley@McKoolSmith.com  
22 **MCKOOL SMITH, P.C.**  
23 300 Crescent Court Suite 1500  
24 Dallas, TX 75201  
25 *\*Pro Hac Applications forthcoming*

26 Attorneys for Plaintiff  
27 BELL SEMICONDUCTOR, LLC

28  
29  
30  
31  
32  
33  
34  
35  
36  
37  
38  
39  
40  
41  
42  
43  
44  
45  
46  
47  
48  
49  
50  
51  
52  
53  
54  
55  
56  
57  
58  
59  
60  
61  
62  
63  
64  
65  
66  
67  
68  
69  
70  
71  
72  
73  
74  
75  
76  
77  
78  
79  
80  
81  
82  
83  
84  
85  
86  
87  
88  
89  
90  
91  
92  
93  
94  
95  
96  
97  
98  
99  
100  
101  
102  
103  
104  
105  
106  
107  
108  
109  
110  
111  
112  
113  
114  
115  
116  
117  
118  
119  
120  
121  
122  
123  
124  
125  
126  
127  
128  
129  
130  
131  
132  
133  
134  
135  
136  
137  
138  
139  
140  
141  
142  
143  
144  
145  
146  
147  
148  
149  
150  
151  
152  
153  
154  
155  
156  
157  
158  
159  
160  
161  
162  
163  
164  
165  
166  
167  
168  
169  
170  
171  
172  
173  
174  
175  
176  
177  
178  
179  
180  
181  
182  
183  
184  
185  
186  
187  
188  
189  
190  
191  
192  
193  
194  
195  
196  
197  
198  
199  
200  
201  
202  
203  
204  
205  
206  
207  
208  
209  
210  
211  
212  
213  
214  
215  
216  
217  
218  
219  
220  
221  
222  
223  
224  
225  
226  
227  
228  
229  
230  
231  
232  
233  
234  
235  
236  
237  
238  
239  
240  
241  
242  
243  
244  
245  
246  
247  
248  
249  
250  
251  
252  
253  
254  
255  
256  
257  
258  
259  
260  
261  
262  
263  
264  
265  
266  
267  
268  
269  
270  
271  
272  
273  
274  
275  
276  
277  
278  
279  
280  
281  
282  
283  
284  
285  
286  
287  
288  
289  
290  
291  
292  
293  
294  
295  
296  
297  
298  
299  
300  
301  
302  
303  
304  
305  
306  
307  
308  
309  
310  
311  
312  
313  
314  
315  
316  
317  
318  
319  
320  
321  
322  
323  
324  
325  
326  
327  
328  
329  
330  
331  
332  
333  
334  
335  
336  
337  
338  
339  
340  
341  
342  
343  
344  
345  
346  
347  
348  
349  
350  
351  
352  
353  
354  
355  
356  
357  
358  
359  
360  
361  
362  
363  
364  
365  
366  
367  
368  
369  
370  
371  
372  
373  
374  
375  
376  
377  
378  
379  
380  
381  
382  
383  
384  
385  
386  
387  
388  
389  
390  
391  
392  
393  
394  
395  
396  
397  
398  
399  
400  
401  
402  
403  
404  
405  
406  
407  
408  
409  
410  
411  
412  
413  
414  
415  
416  
417  
418  
419  
420  
421  
422  
423  
424  
425  
426  
427  
428  
429  
430  
431  
432  
433  
434  
435  
436  
437  
438  
439  
440  
441  
442  
443  
444  
445  
446  
447  
448  
449  
450  
451  
452  
453  
454  
455  
456  
457  
458  
459  
460  
461  
462  
463  
464  
465  
466  
467  
468  
469  
470  
471  
472  
473  
474  
475  
476  
477  
478  
479  
480  
481  
482  
483  
484  
485  
486  
487  
488  
489  
490  
491  
492  
493  
494  
495  
496  
497  
498  
499  
500  
501  
502  
503  
504  
505  
506  
507  
508  
509  
510  
511  
512  
513  
514  
515  
516  
517  
518  
519  
520  
521  
522  
523  
524  
525  
526  
527  
528  
529  
530  
531  
532  
533  
534  
535  
536  
537  
538  
539  
540  
541  
542  
543  
544  
545  
546  
547  
548  
549  
550  
551  
552  
553  
554  
555  
556  
557  
558  
559  
560  
561  
562  
563  
564  
565  
566  
567  
568  
569  
570  
571  
572  
573  
574  
575  
576  
577  
578  
579  
580  
581  
582  
583  
584  
585  
586  
587  
588  
589  
590  
591  
592  
593  
594  
595  
596  
597  
598  
599  
600  
601  
602  
603  
604  
605  
606  
607  
608  
609  
610  
611  
612  
613  
614  
615  
616  
617  
618  
619  
620  
621  
622  
623  
624  
625  
626  
627  
628  
629  
630  
631  
632  
633  
634  
635  
636  
637  
638  
639  
640  
641  
642  
643  
644  
645  
646  
647  
648  
649  
650  
651  
652  
653  
654  
655  
656  
657  
658  
659  
660  
661  
662  
663  
664  
665  
666  
667  
668  
669  
670  
671  
672  
673  
674  
675  
676  
677  
678  
679  
680  
681  
682  
683  
684  
685  
686  
687  
688  
689  
690  
691  
692  
693  
694  
695  
696  
697  
698  
699  
700  
701  
702  
703  
704  
705  
706  
707  
708  
709  
710  
711  
712  
713  
714  
715  
716  
717  
718  
719  
720  
721  
722  
723  
724  
725  
726  
727  
728  
729  
730  
731  
732  
733  
734  
735  
736  
737  
738  
739  
740  
741  
742  
743  
744  
745  
746  
747  
748  
749  
750  
751  
752  
753  
754  
755  
756  
757  
758  
759  
760  
761  
762  
763  
764  
765  
766  
767  
768  
769  
770  
771  
772  
773  
774  
775  
776  
777  
778  
779  
780  
781  
782  
783  
784  
785  
786  
787  
788  
789  
790  
791  
792  
793  
794  
795  
796  
797  
798  
799  
800  
801  
802  
803  
804  
805  
806  
807  
808  
809  
810  
811  
812  
813  
814  
815  
816  
817  
818  
819  
820  
821  
822  
823  
824  
825  
826  
827  
828  
829  
830  
831  
832  
833  
834  
835  
836  
837  
838  
839  
840  
841  
842  
843  
844  
845  
846  
847  
848  
849  
850  
851  
852  
853  
854  
855  
856  
857  
858  
859  
860  
861  
862  
863  
864  
865  
866  
867  
868  
869  
870  
871  
872  
873  
874  
875  
876  
877  
878  
879  
880  
881  
882  
883  
884  
885  
886  
887  
888  
889  
890  
891  
892  
893  
894  
895  
896  
897  
898  
899  
900  
901  
902  
903  
904  
905  
906  
907  
908  
909  
910  
911  
912  
913  
914  
915  
916  
917  
918  
919  
920  
921  
922  
923  
924  
925  
926  
927  
928  
929  
930  
931  
932  
933  
934  
935  
936  
937  
938  
939  
940  
941  
942  
943  
944  
945  
946  
947  
948  
949  
950  
951  
952  
953  
954  
955  
956  
957  
958  
959  
960  
961  
962  
963  
964  
965  
966  
967  
968  
969  
970  
971  
972  
973  
974  
975  
976  
977  
978  
979  
980  
981  
982  
983  
984  
985  
986  
987  
988  
989  
990  
991  
992  
993  
994  
995  
996  
997  
998  
999  
1000

BELL SEMICONDUCTOR, LLC  
Plaintiff,  
v.  
WESTERN DIGITAL  
TECHNOLOGIES, INC.  
Defendant.

**Case No. 8:22-cv-1823**

**ORIGINAL COMPLAINT**

**JURY TRIAL DEMANDED**

ORIGINAL COMPLAINT

1 Plaintiff Bell Semiconductor, LLC (“Bell Semic” or “Plaintiff”) brings this  
2 Complaint against Defendant Western Digital Technologies, Inc. (“Western Digital”)  
3 for infringement of U.S. Patent No. 7,231,626 (“the ’626 patent”). Plaintiff, on personal  
4 knowledge of its own acts, and on information and belief as to all others based on  
5 investigation, alleges as follows:

6 **SUMMARY OF THE ACTION**

7 1. This is a patent infringement suit relating to Western Digital’s  
8 unauthorized and unlicensed use of the ’626 patent. The circuit design methodologies  
9 claimed in the ’626 patent are used by Western Digital in the production of one or more  
10 of its semiconductor chips, including its WD Black SN 850 NVMe SSD (“Western  
11 Digital Accused Product”).

12 2. Traditionally, the process flow for IC design is highly linear, with each phase  
13 of the design process depending on the previous steps. Accordingly, when revisions to  
14 portions of the physical design are made, as typically happens numerous times during  
15 the design process, all the subsequent steps typically need to be redone in their entirety  
16 for at least the layer, if not the entire device. This is because regardless of the size or  
17 extent of the revision to the physical design, the changes must be merged into a much  
18 larger integrated circuit design and then the remaining steps of the design process flow  
19 re-run.

20 3. Before the inventions claimed in the ’626 patent, the typical turnaround time  
21 for implementing a change to the physical design for cutting edge devices was  
22 approximately one week regardless of the size of the change. This is extremely  
23 inefficient in most instances where the change relates to only a small fraction of the  
24 overall design. See Ex. A at 3:16–18 & Fig. 1.

25 4. The ’626 patent’s inventors solved this problem by defining a window that  
26 encloses a change specified by the revision to physical design. The window defines an  
27 area that is less than the area of the entire circuit design. Only the nets within that  
28

1 window are routed pursuant to the revision, leaving the remaining nets in the design  
2 unaffected. Then, the results of that incremental routing are inserted into a copy of the  
3 original IC design to produce a revised IC design that effects the physical design change  
4 without needing to redo the entire process flow.

5 5. Semiconductor devices include different kinds of materials to function as  
6 intended. For example, these devices typically include both metal (*i.e.*, conductor) and  
7 insulator materials, which are deposited or otherwise processed sequentially in layers  
8 to form the final device. These layers—and the interconnects and components formed  
9 within them—have gotten much smaller over time, increasing the performance of these  
10 devices dramatically. As a result, it has become even more important to keep the layers  
11 planar as the device is being built because defects and warpage can cause fabrication  
12 issues and malfunctioning of the device. Manufacturers use a process called Chemical  
13 Mechanical Planarization/Polishing (“CMP”) to smooth out the surface of the device to  
14 prepare the device for further processing, such as deposition of another layer. This  
15 allows subsequent layers to be built and connected more easily with fewer opportunities  
16 for short circuits or other errors that render the device defective. CMP functions best  
17 when there is a certain density and variance of the same material on the surface of the  
18 chip. This is because different materials will be “polished” away at different rates,  
19 leading to erosion or dishing on the surface. To reduce this problem “dummy” material,  
20 also known as “dummy fill,” is typically inserted into low-density regions of the device  
21 to increase the overall uniformity of the structures on the surface of the layer and reduce  
22 the density variability across the surface of the device. However, dummy fill can  
23 increase capacitance if it is placed too close to signal wires, which slows the  
24 transmission speed of signals and degrades the overall performance of the device.

25 6. Bell Semic brings this action to put a stop to Western Digital’s unauthorized  
26 and unlicensed use of the inventions claimed in the ’626 patent.

**THE PARTIES**

7. Plaintiff Bell Semic is a limited liability company organized under the laws of the State of Delaware with a place of business at One West Broad Street, Suite 901, Bethlehem, PA 18018.

8. Bell Semic stems from a long pedigree that began at Bell Labs. Bell Labs sprung out of the Bell System as a research and development laboratory, and eventually became known as one of America's greatest technology incubators. Bell Labs employees invented the transistor in 1947 in Murray Hill, New Jersey. It was widely considered one of the most important technological breakthroughs of the time, earning the inventors the Nobel Prize in Physics. Bell Labs made the first commercial transistors at a plant in Allentown, Pennsylvania. For decades, Bell Labs licensed its transistor patents to companies throughout the world, creating a technological boom that led to the use of transistors in the semiconductor devices prevalent in most electronic devices today.

9. Bell Semic, a successor to Bell Labs' pioneering efforts, owns over 1,900 worldwide patents and applications, approximately 1,500 of which are active United States patents. This patent portfolio of semiconductor-related inventions was developed over many years by some of the world's leading semiconductor companies, including Bell Labs, Lucent Technologies, Agere Systems, and LSI Logic and LSI Corporation ("LSI"). This portfolio reflects technology that underlies many important innovations in the development of semiconductors and integrated circuits for high-tech products, including smartphones, computers, wearables, digital signal processors, IoT devices, automobiles, broadband carrier access, switches, network processors, and wireless connectors.

10. The principals of Bell Semic all worked at Bell Labs' Allentown facility, and have continued the rich tradition of innovating, licensing, and helping the industry at large since those early days at Bell Labs. For example, Bell Semic's CTO was a LSI

1 Fellow and Broadcom Fellow. He is known throughout the world as an innovator with  
2 more than 300 patents to his name, and he has a sterling reputation for helping  
3 semiconductor fabs improve their efficiency. Bell Semic's CEO took a brief hiatus from  
4 the semiconductor world to work with Nortel Networks in the telecom industry during  
5 its bankruptcy. His efforts saved the pensions of tens of thousands of Nortel retirees  
6 and employees. In addition, several Bell Semic executives previously served as  
7 engineers at many of these companies and were personally involved in creating the  
8 ideas claimed throughout Bell Semic's extensive patent portfolio.

9 11. On information and belief, Western Digital has its principal place of  
10 business and headquarters at 5601 Great Oaks Parkway, San Jose, California 95119.

11 12. On information and belief, Western Digital develops, designs, and/or  
12 manufactures products in the United States, including in this District, according to the  
13 '626 patented processes/methodologies; and/or uses the '626 patented  
14 processes/methodologies in the United States, including in this District, to make  
15 products; and/or distributes, markets, sells, or offers to sell in the United States and/or  
16 imports products into the United States, including in this District, that were  
17 manufactured or otherwise produced using the patented process. Additionally, Western  
18 Digital introduces those products into the stream of commerce knowing that they will  
19 be sold and/or used in this District and elsewhere in the United States.

### 20 **JURISDICTION AND VENUE**

21 13. This is an action for patent infringement arising under the Patent Laws of  
22 the United States, Title 35 of the United States Code. Accordingly, this Court has  
23 subject matter jurisdiction under 28 U.S.C. §§ 1331 and 1338(a).

24 14. This Court has personal jurisdiction over Western Digital under the laws  
25 of the State of California, due at least to its substantial business in California and in this  
26 District. Western Digital has purposefully and voluntarily availed itself of the privileges  
27 of conducting business in the United States, in the State of California, and in this  
28

District by continuously and systematically placing goods into the stream of commerce through an established distribution channel with the expectation that they will be purchased by consumers in this District. In the State of California and in this District, Western Digital, directly or through intermediaries: (i) performs at least a portion of the infringements alleged herein; (ii) develops, designs, and/or manufactures products according to the '626 patented process/methodology; (iii) distributes, markets, sells, or offers to sell products formed according to the '626 patented process/methodology; and/or (iv) imports products formed according to the '626 patented processes/methodologies.

15. On information and belief, venue is proper in this Court pursuant to 28 U.S.C. §§ 1391 and 1400 because Western Digital has committed, and continues to commit, acts of infringement in this District and has a regular and established place of business in this District. For example, Western Digital maintains a regular and established place of business in the District at 3355 Michelson Drive, Suite 100, Irvine, CA 92612. Moreover, on information and belief, Western Digital employs nearly 200 engineers in the Irvine area. *See* Search Results for Current Western Digital Employees, LinkedIn (available at [https://www.linkedin.com/search/results/people/?currentCompany=%5B%224593%22%5D&geoUrn=%5B%22103575230%22%5D&keywords=wester n%20digital&origin=FACETED\\_SEARCH&page=13&position=0&searchId=48b4779e-0260-4fdd-a1a0-78d333a8b5fe&sid=q\\_K&title=engineer](https://www.linkedin.com/search/results/people/?currentCompany=%5B%224593%22%5D&geoUrn=%5B%22103575230%22%5D&keywords=wester%20digital&origin=FACETED_SEARCH&page=13&position=0&searchId=48b4779e-0260-4fdd-a1a0-78d333a8b5fe&sid=q_K&title=engineer)) (last visited October 4, 2022).

16. Currently, on information and belief, Western Digital is advertising more than 30 jobs in the Irvine area. These positions include those that relate to the '626 patented technologies, such as positions for a Senior Engineer and Senior Manager, R&D Engineering. *See Careers at Western Digital*, Western Digital (<https://careers.smartrecruiters.com/WesternDigital>) (last visited October 4, 2022).

1 17. Venue is also convenient in this District. This is at least true because of  
2 this District's close ties to this case—including the technology, relevant witnesses, and  
3 sources of proof noted above—and its ability to quickly and efficiently move this case  
4 to resolution.

5 18. On information and belief, Bell Semic's cause of action arises directly  
6 from Western Digital's circuit design work and other activities in this District.  
7 Moreover, on information and belief, Western Digital has derived substantial revenues  
8 from its infringing acts occurring within the State of California and within this District.

9 **U.S. PATENT NO. 7,231,626**

10 19. Bell Semiconductor owns by assignment the entire right, title, and interest  
11 in the '626 patent, entitled "Method Of Implementing An Engineering Change Order  
12 In An Integrated Circuit Design By Windows."

13 20. A true and correct copy of the '626 patent is attached as Exhibit A.

14 21. The '626 patent issued to inventors Jason K. Hoff, Viswanathan  
15 Lakshmanan, Michael Josephides, Daniel W. Prevedel, Richard D. Blinne, and  
16 Johathan P. Kuppinger.

17 22. The application that resulted in issuance of the '626 patent, United States  
18 Patent Application No. 11/015,123, was filed December 17, 2004. It issued on June 12,  
19 2007 and expires on July 26, 2025.

20 23. The '626 patent generally relates to "methods of implementing an  
21 engineering change order (ECO) in an integrated circuit design." Ex. A at 1:1–13.

22 24. The background section of the '626 patent identifies the shortcomings of  
23 the prior art. More specifically, the specification describes that the prior circuit design  
24 methodology was disadvantageous because "[i]n previous methods for implementing  
25 an engineering change order (ECO) request in an integrated circuit design, design tools  
26 are run for the entire integrated circuit design, even though the engineering change  
27  
28



1 order typically is only a small fraction of the size of the integrated circuit design” Ex.  
2 A at 2:15–19.

3 25. The ’626 patent elaborates that because “cell placement, routing, design  
4 rule check validation, and timing closure run times typically scale with the size of the  
5 entire integrated circuit design,” Ex. A at 2:20–22, this produced a “typical turnaround  
6 time” of “about one week regardless of the size of the engineering change order. . . .  
7 because although the engineering change order may only have a size of a few cells, it  
8 must be merged with an integrated circuit design that typically has a much greater size.”  
9 *Id.* at 2:37–44. Certain of these steps “may be especially time consuming and resource  
10 intensive.” *Id.* at 3:16–17.

11 26. The inventions disclosed in the ’626 patent provide many advantages over  
12 the prior art. In particular, they provide a simple and efficient method for ensuring that  
13 revisions to the physical design of the IC do not unduly delay the completion of the  
14 design process. As the ’626 patent explains, “significant savings in the resources  
15 required to perform routing, design rule check verification, net delay calculation, and  
16 parasitic extraction may be realized by creating windows in the integrated circuit design  
17 that include only the incremental changes to the overall integrated circuit design.” Ex.  
18 A at 3:19–23.

19 27. As mentioned above, this is very beneficial because it substantially  
20 reduces the run time of the routing tools and related follow-on steps of the layout  
21 portion of the design process flow (such as calculation of net delay, design rule check,  
22 and parasitic extraction). Thus, it shortens the overall design timeline, and avoids cost  
23 overruns and delays, making it less costly to make changes later in the design process  
24 or more often. *See id.*

25 28. Given the aforementioned increased complexity of circuit designs and the  
26 corresponding delays from design changes, these efficiency gains have become more  
27 and more important in completing the design process without affecting time-to-market.  
28



1 These significant advantages are achieved through the use of the patented inventions  
2 and thus the '626 patent presents significant commercial value for chip designers.

3 29. In light of the drawbacks of the prior art, the '626 patent's inventors  
4 recognized the need for a circuit design methodology in which the time required to  
5 implement an ECO "depend[s] on the number of net changes in the [ECO] rather than  
6 on the total number of nets in the entire integrated circuit design." Ex. A at 2:51–53.  
7 The inventions claimed in the '626 patent address this need.

8 30. The '626 patent contains two independent claims and 8 total claims,  
9 covering a method and computer readable medium for implementing a change order in  
10 an integrated circuit design. Claim 1 reads:

11 1. A method comprising steps of:

12 (a) receiving as input an integrated circuit design;

13 (b) receiving as input an engineering change order to the integrated  
14 circuit design;

15 (c) creating at least one window in the integrated circuit design that  
16 encloses a change to the integrated circuit design introduced by the  
17 engineering change order wherein the window is bounded by  
18 coordinates that define an area that is less than an entire area of the  
integrated circuit design;

19 (d) performing an incremental routing of the integrated circuit  
20 design only for each net in the integrated circuit design that is  
21 enclosed by the window;

22 (e) replacing an area in a copy of the integrated circuit design that  
23 is bounded by the coordinates of the window with results of the  
24 incremental routing to generate a revised integrated circuit design;  
and

25 (f) generating as output the revised integrated circuit design.

26 31. This claim, as a whole, provides significant benefits and improvements to  
27 the function of the semiconductor device design process, *e.g.*, providing a novel and  
28

1 substantially more efficient process flow in which only the affected nets would be  
2 considered in the incremental routing. This results in substantial reduction in the  
3 expected time of the design portion of producing semiconductor devices.

4 32. The claims of the '626 patent also recite inventive concepts that improve  
5 the functioning of the fabrication process, particularly as to post-ECO routing. The  
6 claims of the '626 patent disclose a new and novel solution to specific problems related  
7 to improving semiconductor fabrication. As explained in detail above and in the '626  
8 patent specification, the claimed inventions improve upon the prior art processes by  
9 ignoring nets that are unaffected by an ECO in performing routing following the ECO.  
10 This has the advantage of substantially reducing the impact on design schedule of ECOs  
11 and other layout changes, thus increasing the efficiency of the design process and  
12 making it easier to improve the design and fix design errors without unduly delaying  
13 time-to-market. By making it easier to fix errors as they are found, and causing  
14 substantially less incremental delay upon finding and fixing errors, the claimed  
15 inventive processes also increase the performance and reliability of the finished  
16 product. Because of the claimed inventive processes, individual less impactful design  
17 issues that still impact design performance (albeit not on a critical scale) can be caught  
18 and fixed without costing the same delay as more substantial errors.

19 **COUNT I – INFRINGEMENT OF U.S. PATENT NO. 7,231,626**

20 33. Bell Semic re-alleges and incorporates by reference the allegations of the  
21 foregoing paragraphs as if fully set forth herein.

22 34. The '626 patent is valid and enforceable under the United States Patent  
23 Laws.

24 35. Bell Semic owns, by assignment, all right, title, and interest in and to the  
25 '626 patent, including the right to collect for past damages.

26 36. A copy of the '626 patent is attached at Exhibit A.  
27  
28

1           37. On information and belief, Western Digital has and continues to directly  
2 infringe pursuant to 35 U.S.C. § 271(a) one or more claims of the '626 patent by using  
3 the patented methodology to design one or more semiconductor devices, including as  
4 one example the Western Digital Accused Product, in the United States.

5           38. On information and belief, Western Digital employs a variety of design  
6 tools, for example, Cadence, Synopsys, and/or Siemens tools, to perform incremental  
7 routing in implementing an ECO (the "Accused Processes") as recited in the '626 patent  
8 claims. As one example, Western Digital's Accused Processes perform a method for  
9 only routing the nets affected by the ECO and merging that changed area into the overall  
10 circuit layout as required by claim 1 of the '626 patent. Western Digital does so by  
11 employing a design tool, such as at least one of a Cadence, Synopsys, and/or Siemens  
12 tool, to perform incremental routing as part of implementing an ECO for the Western  
13 Digital Accused Product to generate a revised integrated circuit design.

14           39. Western Digital's Accused Processes also calculate and perform a  
15 parasitic extraction only for each net in the IC design enclosed by the window defining  
16 the ECO. (This parasitic extraction is also how the Accused Processes further calculate  
17 a net delay only for each net in the IC design enclosed by the window defining the  
18 ECO.) Western Digital does so by employing a design tool, such as at least one of the  
19 Cadence, Synopsys, and/or Siemens tools, to perform the incremental routing during  
20 implementation of the ECO for the Western Digital Accused Product's circuit designs.

21           40. Western Digital's Accused Processes also perform a design rule check  
22 only for each net in the IC design enclosed by the ECO window. Western Digital does  
23 so by employing a design tool, such as at least one of the Cadence, Synopsys, and/or  
24 Siemens tools, perform the incremental ECO and automatically perform a DRC for  
25 those nets to ensure that the ECO did not violate any design rules when it fixed other  
26 issues.

1           41. An exemplary infringement analysis showing infringement of one or more  
2 claims of the '626 patent is set forth in Exhibit B. The declaration of Lloyd Linder, an  
3 expert in the field of semiconductor device design, is attached at Exhibit C and further  
4 describes Western Digital's infringement of the '626 patent.

5           42. Western Digital's Accused Processes infringe and continue to infringe one  
6 or more claims of the '626 patent during the pendency of the '626 patent.

7           43. On information and belief, Western Digital has and continues to infringe  
8 pursuant to 35 U.S.C. § 271, *et. seq.*, directly or indirectly, either literally or under the  
9 doctrine of equivalents, by using the Accused Processes in violation of one or more  
10 claims of the '626 patent. Western Digital has and continues to infringe pursuant to 35  
11 U.S.C. § 271, *et. seq.*, directly or indirectly, either literally or under the doctrine of  
12 equivalents, by making, selling, or offering to sell in the United States, or importing  
13 into the United States products manufactured or otherwise produced using the Accused  
14 Processes in violation of one or more claims of the '626 patent.

15           44. Western Digital's infringement of the '626 patent is exceptional and  
16 entitles Bell Semic to attorneys' fees and costs incurred in prosecuting this action under  
17 35 U.S.C. § 285.

18           45. Bell Semic has been damaged by Western Digital's infringement of the  
19 '626 patent and will continue to be damaged unless Western Digital is enjoined by this  
20 Court. Bell Semic has suffered and continues to suffer irreparable injury for which there  
21 is no adequate remedy at law. The balance of hardships favors Bell Semic, and public  
22 interest is not disserved by an injunction.

23           46. Bell Semic is entitled to recover from Western Digital all damages that  
24 Bell Semic has sustained as a result of Western Digital's infringement of the '626  
25 patent, including without limitation and/or not less than a reasonable royalty  
26  
27  
28

**PRAYER FOR RELIEF**

WHEREFORE, Bell Semic respectfully requests that this Court enter judgment in its favor as follows and award Bell Semic the following relief:

- (a) a judgment declaring that Western Digital has infringed one or more claims of the '626 patent in this litigation pursuant to 35 U.S.C. § 271, *et seq.*;
- (b) an award of damages adequate to compensate Bell Semic for infringement of the '626 patent by Western Digital, in an amount to be proven at trial, including supplemental post-verdict damages until such time as Western Digital ceases its infringing conduct;
- (c) a permanent injunction, pursuant to 35 U.S.C. § 283, prohibiting Western Digital and its officers, directors, employees, agents, consultants, contractors, suppliers, distributors, all affiliated entities, and all others acting in privity with Western Digital, from committing further acts of infringement;
- (d) a judgment requiring Western Digital to make an accounting of damages resulting from Infineon's infringement of the '626 patent;
- (e) the costs of this action, as well as attorneys' fees as provided by 35 U.S.C. § 285;
- (f) pre-judgment and post-judgment interest at the maximum amount permitted by law;
- (g) all other relief, in law or equity, to which Bell Semic is entitled.

1 Dated: October 5, 2022

/s/ Alan P. Block

2 Alan P. Block (SBN 143783)

3 ablock@mckoolsmith.com

**MCKOOL SMITH, P.C.**

4 300 South Grand Avenue, Suite 2900

5 Los Angeles, California, Suite 2900

6 Telephone: (213) 694-1200

Facsimile: (213) 694-1234

7 Paul Richter\*

8 **DEVLIN LAW FIRM LLC**

9 1526 Gilpin Avenue

10 Wilmington, Delaware 19806

11 Telephone: (302) 449-9010

Facsimile: (302) 353-4251

12 David Sochia\*

13 dsochia@McKoolSmith.com

Ashley N. Moore\*

14 amoore@McKoolSmith.com

15 Richard A. Kamprath\*

rkamprath@McKoolSmith.com

16 Alexandra Easley\*

17 aeasley@McKoolSmith.com

**MCKOOL SMITH, P.C.**

18 300 Crescent Court Suite 1500

19 Dallas, TX 75201

20 *\*Pro Hac Vice Applications forthcoming*

21 *Attorneys for Plaintiff Bell Semiconductor,*  
22 *LLC*

**DEMAND FOR JURY TRIAL**

Plaintiff hereby demands a jury trial for all issues so triable.

Dated: October 5, 2022

/s/ Alan P. Block

Alan P. Block (SBN 143783)

ablock@mckoolsmith.com

**MCKOOL SMITH, P.C.**

300 South Grand Avenue, Suite 2900

Los Angeles, California, Suite 2900

Telephone: (213) 694-1200

Facsimile: (213) 694-1234

Paul Richter\*

**DEVLIN LAW FIRM LLC**

1526 Gilpin Avenue

Wilmington, Delaware 19806

Telephone: (302) 449-9010

Facsimile: (302) 353-4251

David Sochia\*

dsochia@McKoolSmith.com

Ashley N. Moore\*

amoore@McKoolSmith.com

Richard A. Kamprath\*

rkamprath@McKoolSmith.com

Alexandra Easley\*

aeasley@McKoolSmith.com

**MCKOOL SMITH, P.C.**

300 Crescent Court Suite 1500

Dallas, TX 75201

*\*Pro Hac Vice Applications forthcoming*

*Attorneys for Plaintiff Bell Semiconductor,  
LLC*